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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Application Number	10/648,474
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		First Named Inventor	Morgenshtein
		Group Art Unit	2819
		Examiner Name	
Sheet	2	Of	2
		Attorney Docket Number	26327
OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
JC		Al-Assadi et al, "Pass-Transistor Logic Design", <i>Int. J. Electronics</i> , 70(4):739-749, 1991	
JC		Chandrakasan et al, "Minimizing Power Consumption in Digital CMOS Circuits", <i>Proc. IEEE</i> , 83(4):498-523, 1995	
JC		Ozdag et al, "High-Speed QDI Asynchronous Pipelines", <i>Proc. 8th Int. Symposium on Asynchronous Circuits and Systems</i> , April, 2002, pp. 1-10	
JC		Morgenshtein et al, "Gate-Diffusion Input (GDI) – A Novel Power Efficient Method for Digital Circuits: A Design Methodology", <i>14th Annual IEEE International ASIC/SOC Conference</i> , Sept., 2001, pp. 39-43	
JC		Morgenshtein et al, "Gate-Diffusion Input (GDI): A Power Efficient Method for Digital Combinatorial Circuits", <i>IEEE Trans. VLSD Systems</i> , 10(5):566-581, Oct., 2002	
JC		Morgenshtein et al, "Asynchronous exaggerate Gate-Diffusion Input (GDI) Circuits", <i>ISCAS 2002 IEEE International Symposium on Circuits and Systems</i> , May, 2002, pp. 1-8	
JC		David et al, "An Efficient Implementation of Boolean Functions as Self-Timed Circuits", <i>IEEE Trans. On Computers</i> , 41(1):2-11, 1992	
JC		Alidina et al, "Precomputation-Based Sequential Logic Optimization for Low Power", <i>IEEE Trans. VLSD Systems</i> , 2(4):426-436, 1994	
JC		Zimmerman et al, "Low-Power Logic Styles: CMOS Versus Pass-Transistor Logic", <i>IEEE J. Solid-State Circuits</i> , 32(7):1079-1090, 1997	
JC		Yano et al, "Top-Down Pass-Transistor Logic Design", <i>IEEE J. Solid-State Circuits</i> , 31(6):792-803, 1996	
JC		Chandrakasan et al, "Low-Power CMOS Digital Design", <i>IEEE J. Solid-State Circuits</i> , 27(4):473-484, 1992	
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